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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,310	11/23/2004	Roman Woyzichovski	10901/81	6114

26646 7590 07/20/2007
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EXAMINER	
PERILLA, JASON M	
ART UNIT	PAPER NUMBER
2611	
MAIL DATE	DELIVERY MODE
07/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/501,310	WOYZICHOVSKI, ROMAN	
	Examiner	Art Unit	
	Jason M. Perilla	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 July 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 21-40 are pending in the instant application.

Information Disclosure Statement

2. The information disclosure statement filed July 12, 2004 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but some of the information referred to therein has not been considered. The Examiner has considered the U.S. Patent documents and the initialed foreign documents but not the foreign documents without initials because no copy of those documents was provided.

Specification

3. The disclosure is objected to because of the following informalities: In conjunction with the drawing objections set forth below, the paragraph of the specification starting on line 30 of page 7 should be amended to be more consistent with the drawings. Specifically, the statement that "the values of string of results d are supplied from assignment unit 4 in combination unit 8 to a filter" should be amended to more clearly describe the invention according to figure 1. Clearly, the string of results d is not supplied by the assignment unit 4 and the assignment unit 4 is not "in" combination unit 8.

Appropriate correction is required.

Drawings

4. The drawings are objected to because,

a. the reference blocks contain no text labels consistent with the specification and

b. the same reference numerals are used for different functional blocks.

Specifically, with reference to (b) above, reference 4 of the figure designates 3 assignment units which output, respectively, k1, k2, and k3. However, in the specification, k1 and k2 are referred to as "correctional values" and k3 is referred to as a "quality criterion" (see pg. 7). Because these "assignment units" output different types of information, they are considered to perform different functions and should be provided with different reference numerals.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claims 21-40 are objected to because of the following informalities:

The following versions of claims 21 and 40 are presented by the Examiner to overcome objections to the claims.

21. A method for interpolating at least two position-dependent, periodic analog signals that are phase-shifted with respect to one another and which are generated by scanning a measuring scale, comprising:

converting each of the analog signals into a digital data stream by a sigma- delta modulator;

generating a string of results by combining the data streams with correctional ~~factors~~ values and subsequently combining the data streams with one another;

generating from the string of results ~~(a) new correctional values~~ a combination output in accordance with a quality criterion that is to be satisfied during interpolation ~~and (b) output signals of the interpolation~~;

accumulating over a specifiable time interval values of the ~~string of results~~ combination output for generating the correctional values and ~~the~~ output signals; and

using a signal sequence generated by the accumulation as an address sequence for generating the correctional values and for generating the output signals.

40. A device for interpolating at least two position-dependent, periodic analog signals that are phase-shifted with respect to each other and which are generated by scanning a measuring scale, comprising:

a sigma-delta modulator configured to convert the analog signals to a respective digital data stream;

an arithmetic unit configured to generate a string of results in accordance with a combination of the data streams with correctional ~~factors~~ values and ~~in accordance with~~ subsequent combination of the data streams with one another;

an arrangement configured to generate, from the string of results~~, (a) new correctional values~~ a combination output in accordance with a quality criterion that is to be satisfied during the interpolation ~~and (b) output signals of the interpolation~~;

a filter configured to accumulate values of the ~~string of results~~ combination output over a specified time interval to generate an address sequence to control the arithmetic unit to guide the string of results to satisfy the quality criterion; and

an evaluation circuit post-connected to the filter configured to convert address values of the address sequence into output values of the interpolation.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 28 and 29 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 28, the claim is indefinite because one skilled in the art is unable to determine what constitutes a "high value" part of the address sequence. Further, one is unable to determine what an "integral part" of the address value is.

Regarding claim 29, the claim is indefinite for the same reasons as applied to claim 28 above.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 21-24, 26, 27, and 30-40 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Liessner (U.S. Pat. No. 5079549) in view of Garverick et al (U.S. Pat. No. 5134578; "Garverick").

Regarding claim 21, Liessner discloses a method for interpolating (col. 2, lines 20-25) at least two position-dependent, periodic analog signals (fig. 1, SIN(X), COS(X)) that are phase-shifted with respect to one another and which are generated by scanning a measuring scale (abstract), comprising: generating a string of results (fig. 1, "ERROR SIGNAL") by combining (fig. 1, ref. 20) the periodic analog signals with correctional values (fig. 1, outputs of 16 and 18) and subsequently combining the periodic analog signals with one another; generating from the string of results a combination output (fig. 1, output of ref. 24; "UP" and "DOWN") in accordance with a quality criterion (fig. 1, output of error "DETECTOR"; "ES>0" or "ES<0") that is to be satisfied during interpolation (col. 3, lines 40-55); accumulating (fig. 1, ref. 24; fig. 4A, refs. 25 and 27) over a specifiable time interval (according to disable pulse generator, i.e. fig. 4A, ref. 29)

values of the combination output for generating the correctional values (outputs of fig. 1, refs. 16 and 18) and output signals (fig. 1, "Y"); and using a signal sequence generated by the accumulation as an address sequence (also fig. 1, "Y") for generating the correctional values and for generating the output signals (fig. 1). Liessner discloses that the multipliers or combiners (fig. 1, refs. 12 and 14) which combine the periodic analog signals (fig. 1, SIN(X), COS(X)) with correctional values (fig. 1, outputs of 16 and 18) are "multiplying digital to analog converters that cause a digital input to attenuate an analog signal" (col. 3, lines 25-30). Therefore, the outputs from the lookup tables (fig. 1, refs. 16 and 18) are digital and the periodic signals (fig. 1, SIN(X), COS(X)) are analog ones which are attenuated according to the outputs from the lookup tables. Liessner does not explicitly disclose using sigma-delta modulators to convert the periodic analog signals into digital signals. However, it would have been obvious to one having ordinary skill in the art that the analog/digital converting function could be separated from the combining function in each multiplier/combiner (fig. 1, refs. 12 and 14) of Liessner. Furthermore, the use of sigma-delta analog to digital converters is notoriously known in the art as evidenced by Garverick. Garcerick discloses the use of several sigma-delta analog to digital converters (fig. 1, refs. 21-26) to convert various phases of an analog signal into digital form (col. 4, lines 14-20). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the multiplier/combiners of Liessner could be replaced by separate sigma delta analog to digital converters

as suggested by Garverick and purely digital combiners because the use of sigma-delta converters and a fully digital implementation of the invention of Liessner would be widely accepted as advantageous in the art.

Regarding claims 22 and 23, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, as broadly as claimed, Liessner's counter (fig. 1, ref. 24) is considered to be both a filter and an integrator because its output depends upon an accumulation of the past inputs.

Regarding claim 24, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further. Liessner discloses forming the address sequence (fig. 1, "Y") from the accumulation (fig. 1, ref. 24), the address sequence including address values that represent phase information of the analog signals (col. 3, lines 35-40).

Regarding claim 26, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further. Liessner discloses that the address values are a linear function of the phases of the periodic signals when the quality criterion is satisfied. The address values are a linear function of the phases because the error of phases directly determine the address values in a linear fashion (col. 4, lines 19-38).

Regarding claim 27, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further. Liessner discloses that the address sequence (fig. 1, "Y") represent a phase value having a fractional proportion (col. 3, lines 35-40).

Regarding claim 30, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses that the generation of new correctional values is in accordance with the quality criterion (amount of error) until it is satisfied because the embodiment is a closed loop embodiment (fig. 1).

Regarding claim 31, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses storing possible correction values as predefined values in an assignment unit (col. 3, lines 35-40).

Regarding claim 32, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses the remaining limitations of the claim as applied in claim 21 above.

Regarding claim 33, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses that the correctional values correspond to values of a trigonometric function (col. 3, lines 35-40).

Regarding claim 34, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses that the analog signals are phase shifted by 90 degrees with respect to each other as applied in claim 21 above.

Regarding claim 35, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses that the analog signals are substantially sinusoid as applied in claim 21 above.

Regarding claim 36, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, Liessner discloses the remaining limitations of the claim as applied to claim 21 above. Liessner discloses adding (fig. 1, ref. 20) subsequent to multiplying (fig. 1, refs. 12 and 14).

Regarding claim 37, Liessner in view of Garverick disclose the limitations of claim 21 as applied above. Further, it is inherent that a piece of data may have a word width of one bit as understood by one having ordinary skill in the art.

Regarding claim 38, Liessner in view of Garverick disclose the limitations of claim 36 as applied above. Further, Liessner discloses the remaining limitations of the claim as applied to claim 21 above. Liessner discloses adding (fig. 1, ref. 20) subsequent to reducing or attenuating (fig. 1, refs. 12 and 14; col. 3, lines 25-30; "attenuating").

Regarding claim 39, Liessner in view of Garverick disclose the limitations of claim 38 as applied above. Further, Liessner discloses combining by addition (fig. 1, ref. 20) the correctional values. Furthermore, in the purely digital implementation of Liessner in view of Garverick, the addition of the correctional values would result in one of four possibilities as understood by one having ordinary skill in the art because no other possibilities could exist.

Regarding claim 40, Liessner in view of Garverick disclose the limitations of the claim as applied to claim 21 above.

10. Claim 25 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Liessner in view of Garverick, and in further view of The Applicant's Admitted Prior Art ("AAPA").

Regarding claim 25, Liessner in view of Garverick disclose the limitations of claim 24 as applied above. Liessner does not explicitly disclose that the output signals (fig. 1, "Y") are generated from the address sequence by low- pass filtering and assignment of the address values. However, low-pass filtering and assignment of the address values is well known in the art as evidenced in the discussion of the AAPA (page 2, lines 7-10). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made that the address sequence of Liessner could be fed through a low-pass filter (i.e. within UP/DOWN counter 26 of figure 1) as suggested by the AAPA because it was a well known method in the art.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following prior art of record not relied upon above is cited to further show the state of the art with respect to interpolators.

U.S. Pat. No. 4462083 to Schwefel.

U.S. Pat. No. 5786781 to Taniguchi et al.

U.S. Pat. No. 6608573 to Kushihara.

U.S. Pat. No. 6278388 to Kushihara.

U.S. Pat. No. 4225931 to Schwefel.

U.S. Pat. No. 4987414 to Iijima at al.

U.S. Pat. No. 6041336 to Steinlechner.

U.S. Pat. No. 5943639 to Tanaka et al.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jason M. Perilla
July 18, 2007

jmp

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER